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10/651,599	08/29/2003	Raymond A.. Davis	MICR-155US	9701

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RATNERPRESTIA
P.O. BOX 980
VALLEY FORGE, PA 19482

EXAMINER	
LAM, HUNG H	
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/651,599	DAVIS, RAYMOND A..	
	Examiner	Art Unit	
	HUNG H. LAM	2622	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11 February 2009*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-35 and 39-41* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-35 and 39-41* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *08/29/03* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

1. The amendments, filed on 02/11/09, have been entered and made of record. Claim 36-37 are canceled. Claims 1-35 and 38-41 are pending.

Allowable Subject Matter

2. The indicated allowability of claims 1-35 and 38-41 are withdrawn in view of the newly discovered reference(s) to Shirakawa. Rejections based on the newly cited reference(s) follow.

3. Therefore, the Final Office Action mailed on 02/11/09 has been vacated/withdrawn and replaced by this Non Final Office Action.

Claim Rejections - 35 USC § 102

4. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

5. Claims 17-21 and 26-35 and 38-40 are rejected under 35 U.S.C. 102(b) as being anticipated by Shirakawa (US-2003/0,117,501).

Regarding **claim 17**, Shirakawa discloses an electronic apparatus comprising:

a substrate having circuitry thereon for receiving image data (Figs. 1 and 9; it is inherent that Front and Back camera 10b-10a module include circuitry on a board and/or substrate); and

a dual camera module connected to said substrate, said dual camera module adapted to capture images (Fig. 2; camera module 1; abstract), the dual camera module including a first image module (2a) adapted to capture a first image in a first direction (back ground or Back Camera), and including a first output for transmitting the first captured image to the circuitry on the substrate (see Sa-Sb output; [0030-0031]),a second image module (2b) adapted to capture second image in a second direction (User's face or Front Camera), and including a second output for transmitting the second captured image to the circuitry on the substrate (see Sa-Sb output; [0030-0031]) , and

a common set of data lines that are shared by the first and second image modules (see line connection from switch 5 to DSP 3), the common set of data lines being configured to electrically connect the first and second outputs to the circuitry on the substrate (see line connection from switch 5 to DSP 3 and Sa-Sb and camera module 1), wherein, at the first image module, a portion of the first captured image (2a) is selectively blocked by tri-stating a connection between the first image module and the common set of data lines during a first time period (see switch 5; [0033]) and at the second image module (2b), a portion of the second captured image is selectively blocked by tri-stating a connection between the second image module and the common set of data lines during a second time period ([0033]), the first and second time periods

being consecutive time periods to synchronize the first and second captured images ([0032-0033]) received by the circuitry on the substrate to generate a composite image that includes at least one portion of each of the captured first and second images ([0034-0037]).

Regarding **claim 18**, Shirakawa discloses the electronic apparatus recited in claim 1, wherein each of the image modules comprises a lens and an imaging sensor (Shirakawa: see Fig. 1).

Regarding **claim 19**, Shirakawa discloses the electronic apparatus recited in claim 1, wherein each of the image modules comprises a lens and a combination imaging sensor and image processor (Fig 5; wherein Shirakawa further teaches each front and back camera include DSP 3b-3a).

Regarding **claim 20**, Shirakawa discloses the electronic apparatus recited in claim 17, wherein each of the image modules further comprises an imaging filter ([0031]).

Regarding **claim 21**, Shirakawa discloses the electronic apparatus recited in claim 17, wherein the first direction and the second direction are opposite directions relative to each other (see Fig. 2: [0029-0031]).

Regarding **claim 26**, Shirakawa discloses the electronic apparatus recited in claim 17, wherein the image modules respond to a common address ([0044]: Shirakawa further teaches camera 1a and 1b connected to a common bus 8. Therefore, both cameras inherently respond to an address).

Regarding **claim 27**, Shirakawa discloses the electronic apparatus recited in claim 17, further comprising: a screen for displaying the composite image (see Fig. 3C-4B).

Regarding **claim 28**, Shirakawa discloses the electronic apparatus recited in claim 17, further comprising: a screen coupled to the circuitry on the substrate for displaying the composite image which includes one of: (1) the first and second captured images synchronized to generate a split screen orientation thereof for display, or (2) the first and second captured images synchronized to generate a picture-in-picture orientation thereof for display (see Fig. 3C-4B: [0037-0038]).

Regarding **claim 29**, Shirakawa discloses the electronic apparatus recited in claim 17, wherein said first image module has a first focal length and said second image module has a second focal length ([0031]).

Regarding **claim 30**, Shirakawa discloses the electronic apparatus recited in claim 17, wherein the first image module captures images of a first resolution and the second image module captures images of a second resolution ([0030]).

Regarding **claim 31**, Shirakawa discloses an electronic apparatus, comprising:

a substrate (Figs. 1 and 9; it is inherent that Front and Back camera 10b-10a module include a board and/or substrate);

a first image module adapted to capture a first image with a first orientation in a first direction and mounted on said substrate (see Figs. 2 and 9; [0030-0031]);

a second image module adapted to capture a second image with a second orientation in either the first direction or in a second direction and mounted on said substrate (see Figs. 2 and 9; [0030-0031]), and

a screen coupled to the substrate and adapted to display the first and second images captured by said first and second image modules (Fig. 9; display 92), wherein, at the first image module, a portion of the first captured image is selectively blocked by tri-stating an output thereof during a first time period and at the second image module (see switch 5; [0033]), a portion of the second captured image is selectively blocked by tri-stating an output thereof during a second time period (see switch 5; [0032-0033]), the first and second time periods being consecutive time periods to synchronize the first and second captured images received by circuitry on the substrate to generate a composite image of at least one portion of each of the first and

second images on the screen (Figs. 3C-4B; [0034-0038]).

Regarding **claim 32**, Shirakawa discloses the electronic apparatus recited in claim 17, further comprising: a screen for displaying the composite image (Figs. 3C-4B).

Regarding **claim 33**, Shirakawa discloses the electronic apparatus recited in claim 31, wherein each of the image modules comprises a lens and an imaging sensor (see Fig. 2).

Regarding **claim 34**, Shirakawa discloses the electronic apparatus recited in claim 31, wherein each of the image modules is a combination sensor and image processor (Fig. 6; [0042-0043]).

Regarding **claim 35**, Shirakawa discloses the electronic apparatus recited in claim 31, wherein said first image module faces the first direction and said second image module faces the second direction (Fig. 2; [0029-0031]).

Regarding **claim 38**, Shirakawa discloses a method of operating an electronic apparatus, the electronic apparatus including first and second image modules having first and second outputs (abstract), respectively, said method comprising

capturing first and second scenes, as first and second data streams, using the first image module and the second image module (abstract; [0014; 0028-0030]), respectively;

transmitting the first image data stream to circuitry on a substrate via at least one common data line (see line connection from switch 5 to DSP 3) and the first output of the first image module ([0014; 0028-0030]);

transmitting the second image data stream to the circuitry on the substrate via the at least one common data line (see line connection from switch 5 to DSP 3) and the second output of the second image module ([0014; 0028-0030]); and

synchronizing the first and second image data streams received by the circuitry on the substrate by selectively blocking reception of portions of the first and second image data streams transmitted by the first and second outputs ([0032-0033]),respectively, via the at least one common data line to the circuitry on the substrate, to generate a composite image data stream ([0014; 0028-0037]), wherein the synchronizing of the first and second image data includes tri-stating an output of the first image module during a first time period and tri-stating an output of the second image module during a second time period ([0014; 0028-0037]), the first and second time periods being consecutive time periods such that the first and second captured image data received by the circuitry on the substrate are synchronized to generate the composite image data stream including at least one portion of each of the first and second image data ([0036-0038]).

Regarding **claim 39**, Shirakawa the method recited in claim 38 wherein the at least one common data line is included in a shared tri-state bus and the synchronizing of the first and second image data stream includes selectively tri-stating the first and second outputs using the shared tri-state bus to generate the composite image data stream ([0014; 0028-0037]).

Regarding **claim 40**, Shirakawa the method recited in claim 38, wherein the synchronizing of the first and second image data streams is based on a portion of the first scene defining a window-of-disinterest ([0036-0038]).

Claim Rejections - 35 USC § 103

6. Claims 1-7, 11-16 and 41 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shirakawa (US-2003/0,117,501) in view of Miyake (US-2001/0,050,721).

Regarding **claim 1**, Shirakawa discloses a dual camera module comprising:

a substrate having circuitry thereon for receiving image data (Figs. 1 and 9; it is inherent that Front and Back camera 10b-10a module include circuitry on a board and/or substrate);

a first image module (2a) for capturing first image data of a first orientation of a first scene (back ground or Back Camera), and including a first output for transmitting the first image data to the circuitry on the substrate (see Sa-Sb output; [0030-0031]);

a second image module (2b) for capturing second image data of a second orientation of the first scene, different from the first orientation of the first scene, or a different scene (User's face or Front Camera), and including a second output for transmitting the second image data to the circuitry on the substrate (see Sa-Sb output; [0030-0031]); and

an interconnect having a common data line that is shared by the first and second image modules (see line connection from switch 5 to DSP 3), the common data line being configured to electrically connect the first and second outputs (Sa-Sb) to the circuitry on the substrate (see line connection from switch 5 to DSP 3 and Sa-Sb and camera module 1),

wherein, at the first image module, a portion of the first image data is selectively blocked by tri-stating a connection between the first image module (2a) and the common data line (see line connection from switch 5 to DSP 3) during a first time period (see switch 5; [0033]) and at the second image module, a portion of the second image data is selectively blocked by tri-stating a connection between the second image module and the common data line (see line connection from switch 5 to DSP 3) during a second time period (see switch 5; [0033]), the first and second time periods being consecutive time periods to synchronize the first and second image data received by the circuitry on the substrate (0032-0034) to generate a composite image that includes at least one portion of each of the captured first and second image data ([0034-0037]).

However, Shirakawa fails to explicitly disclose the interconnect line is a flex interconnect line.

In the same field of endeavor, Miyake teaches a dual camera module that attached to a flex printed circuit or connector ([0161-0162; 0236]). In light of the teaching from Miyake, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the device of Shirakawa with a flex line data bus in order to simplify a design. The modifications thus provide more flexibility to the dual camera module.

Regarding **claim 2**, Shirakawa in view of Miyake discloses the dual camera module recited in claim 1, further comprising: control lines, further data lines and at least one component on the flex interconnect that are shared by the first and second image modules(Miyake: [0236]: it is inherent that sharing control and data lines and at least one component are on the flexible printed circuit).

Regarding **claim 3**, Shirakawa in view of Miyake discloses the dual camera module recited in claim 1, wherein each of the image modules comprises a lens and an imaging sensor (Shirakawa: see Fig. 1).

Regarding **claim 4**, Shirakawa in view of Miyake discloses the dual camera module recited in claim 1, wherein each of the image modules comprises a lens and a combination imaging sensor and image processor (Fig 5; wherein Shirakawa further teaches each front and back camera include DSP 3b-3a).

Regarding **claim 5**, Shirakawa in view of Miyake discloses the dual camera module recited in claim 1, wherein the first image module faces a first direction and the second image module faces a second direction such that the first image data represents the first scene and the second image data represents the different scene (Shirakawa: see Figs. 1, 5 and 9).

Regarding **claim 6**, Shirakawa in view of Miyake discloses the dual camera module recited in claim 1, wherein each of the image modules is uniquely addressable (Shirakawa: Fig. 1; switch 5 is interpreted as a way of address to cameras 10a-10b. Further more, Shirakawa : [0044] further teaches an embodiment in Fig. 7 wherein each camera connected to bus 8. Therefore, it is inherent that each camera is uniquely addressable; Miyake: [0161-0162; 0236]: each camera inherently addressable in order for the dual image sensor to work).

Regarding **claim 7**, Shirakawa in view of Miyake discloses the dual camera module recited in claim 1, wherein the first and second image modules respond to a common or global address (Shirakawa : [0044]; Miyake: [0161-0162; 0236]).

Regarding **claim 11**, the claim contains the same limitations as claimed in claim 7. Therefore, claim 11 is analyzed and rejected as claim 7.

Regarding **claim 12**, Shirakawa in view of Miyake discloses the dual camera module wherein the first and second image modules are each configured to tri-state an output signals (Shirakawa: Fig. 2; see Switch 5).

Regarding **claim 13**, Shirakawa in view of Miyake discloses the dual camera wherein a first image module captures images at a first resolution and the second image module captures images at a second resolution (Shirakawa: [0030]; Miyake: Figs. 22A-22B; 0161-0162: it is inherent that both image sensors 2 capture images at first and second resolution).

Regarding **claim 14**, Shirakawa in view of Miyake discloses the dual camera module wherein a first image module captures images having a first orientation and a second image module captures images having a second orientation (Shirakawa: see Figs. 1, 5 and 9; Miyake: see Figs. 22A-22B; 0161-0162).

Regarding **claim 15**, Shirakawa in view of Miyake discloses the dual camera module recited in claim 1, wherein the first image module captures images of a first color range and the second image module captures images of a second color range (Shirakawa : [0030])

Regarding **claim 16**, Shirakawa in view of Miyake discloses the dual camera module recited in claim 1, wherein the first image module has a first focal length and a second image module has a second focal length (Shirakawa : [0030-0031]).

Regarding **claim 41**, Shirakawa in view of Miyake discloses the dual camera module recited in claim 1, wherein: the first and second image modules have a shared, common housing and include first and second imaging arrays (Shirakawa: see Figs. 2 and 9; Miyake: 0161-0162; 0236), respectively; and

the flex interconnect attaches the shared, common housing to the substrate and electrically connects the first and second imaging arrays to the circuitry of the substrate (Miyake: see Figs. 22A-22B).

7. Claims 8 and 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shirakawa (US-2003/0,117,501) in view of Miyake (US-2001/0,050,721) and further in view of Johnson (US-2006/0,197,847).

Regarding **claim 8**, Shirakawa in view of Miyake fails to disclose the dual camera module recited in claim 1, wherein said flex interconnect includes an Inter-IC (I2C) bus.

In the same field of endeavor, Johnson teaches an image processor system wherein I2C bus is used for allowing multiple cameras to be connected together (0128). Johnson further teaches that a respective data processing subsystem includes

registers, which are configured according to the present invention to share a common address space (0014). In light of the teaching from Johnson, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the device of Shirakawa and Miyake by including an I2C bus in a flexible printed circuit board in order to allow multiple cameras to be connected together and thereby simplify camera circuitry.

Regarding **claim 10,** Shirakawa in view of Miyake fails disclose the dual camera module wherein each of the image modules is programmed to respond to a unique Inter-IC (I2C) address

In the same field of endeavor, Johnson teaches an image processor system wherein I2C bus is used for allowing multiple cameras to be connected together (0128). Johnson further teaches that a respective data processing subsystem includes registers, which are configured according to the present invention to share a common address space (0014; 0128: it is inherent that each camera is programmed with a unique I2C address in order to distinguish each one of the multiple cameras). In light of the teaching from Johnson, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the device of Shirakawa and Miyake by including an I2C bus in a flexible printed circuit board in order to allow multiple cameras to be connected together and thereby simplify camera circuitry.

8. Claims 9 and 22-25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shirakawa in view of Miyake and further in view of Stam (US-2004/0,230,358).

With regarding **claim 9**, Shirakawa in view of Miyake fails to disclose the dual camera module wherein said flex interconnect includes a Serial Peripheral Interface (SPI).

In the same field of endeavor, Stam teaches image sensor side LVDS transceivers which are integrated into an imager (Fig. 9c; 901c) along with other components (0260). This integration thus reduces the part count, component cost and imager board area associated with image sensor side LVDS transceivers (0260). Stam further teaches that the communication protocols such that a serial bus, LVDS serial bus, SPI bus or IIC bus may be used to transmit data from the imager to the processor or from the processor to the imager (0260). In light of the teaching from Stam, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the device of Shirakawa and Miyake by integrating a serial bus, LVDS serial bus, SPI bus or IIC into an imager along with other components. The modifications thus reduce the part count, components cost and imager board area and provide communication between imager and processor (Stam: 0260).

Regarding **claim 22,** Shirakawa fails disclose the electronic apparatus recited in claim 17, wherein said common set of data lines is included in a flex interconnect.

However, Shirakawa fails to explicitly disclose the interconnect line is a flex interconnect line.

In the same field of endeavor, Miyake teaches a dual camera module that attached to a flex printed circuit or connector ([0161-0162; 0236]). In light of the teaching from Miyake, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the device of Shirakawa with a flex line data bus in order to simplify a design. The modifications thus provide more flexibility to the dual camera module.

However, Shirakawa in view of Miyake fails to disclose a flex interconnect that includes an Inter-Integrated Circuit (I2C) bus.

In the same field of endeavor, Stam teaches image sensor side LVDS transceivers which are integrated into an imager (Fig. 9c; 901c) along with other components (0260). This integration thus reduces the part count, component cost and imager board area associated with image sensor side LVDS transceivers (0260). Stam further teaches that the communication protocols such that a serial bus, LVDS serial bus, SPI bus or IIC bus may be used to transmit data from the imager to the processor or from the processor to the imager (0260). In light of the teaching from Stam, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the device of Shirakawa and Miyake by integrating a serial bus, LVDS serial bus, SPI bus or IIC into an imager along with other components. The modifications thus reduce the part count, components cost and imager board area and provide communication between imager and processor (Stam: 0260).

Regarding **claim 23,** Shirakawa fails disclose the electronic apparatus recited in claim 17, wherein said common set of data lines is included in a flex interconnect.

In the same field of endeavor, Miyake teaches a dual camera module that attached to a flex printed circuit or connector ([0161-0162; 0236]). In light of the teaching from Miyake, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the device of Shirakawa with a flex line data bus in order to simplify a design. The modifications thus provide more flexibility to the dual camera module.

However, Shirakawa in view of Miyake fails to disclose a flex interconnect that includes a Serial Peripheral Interface (SPI) bus.

In the same field of endeavor, Stam teaches image sensor side LVDS transceivers which are integrated into an imager (Fig. 9c; 901c) along with other components (0260). This integration thus reduces the part count, component cost and imager board area associated with image sensor side LVDS transceivers (0260). Stam further teaches that the communication protocols such that a serial bus, LVDS serial bus, SPI bus or IIC bus may be used to transmit data from the imager to the processor or from the processor to the imager (0260). In light of the teaching from Stam, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the device of Shirakawa and Miyake by integrating a serial bus, LVDS serial bus, SPI bus or IIC into an imager along with other components. The modifications

thus reduce the part count, components cost and imager board area and provide communication between imager and processor (Stam: 0260).

Regarding **claim 24,** Shirakawa in view of Miyake and further in view of Stam discloses the electronic apparatus recited in claim 22, wherein each of the image modules is programmed to respond to a unique I2C address (Stam: 0048; 0163; 0260).

Regarding **claim 25,** Shirakawa in view of Miyake and further in view of Stam discloses the electronic apparatus recited in claim 23, wherein each of the image modules is programmed to respond to a unique slave select signal on the SPI bus (Stam: [0168; 0256-02567]).

Conclusion

9. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

a) Sasa (US-7,024,041) discloses a tri-state switch for switching between reference image generating circuit and other imaging apparatus.

b) Sawyer (US-5,321,772) discloses a tri-state buffer that permit selective gating of parallel outputs of an association shift register onto a data-bus.

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to HUNG H. LAM whose telephone number is (571)272-7367. The examiner can normally be reached on Monday - Friday 8AM - 5PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, SINH TRAN can be reached on 571-272-7564. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

HL
04/12/09

/M. Lee/
Primary Examiner, Art Unit 2622